IN THE SPECIFICATION

1. On page 1, lines 5-11 of the specification, please amend the text as follows:

-- This application claims priority to U.S. Provisional Patent Application Serial No. 60/134,253 filed May 13, 1999, entitled "Method And Apparatus For Synthesizing And Implementing Integrated Circuit Designs," and to co-pending U.S. Patent Application No. 09/418,663 filed October 14, 1999, entitled "Method And Apparatus For Managing The Configuration And Functionality Of A Semiconductor Design," now U.S. Patent No. 6,862,563, which claims priority to U.S. Provisional Patent Application Serial No. 60/104,271 filed October 14, 1998, of the same title.--

2. On page 13, lines 21-27 of the specification, please amend the text as follows:

-- Referring now to Fig. 4, the method 400 of synthesizing logic incorporating the jump delay slot mode functionality previously discussed is described. The generalized method of synthesizing integrated circuit logic having a user-customized (i.e., "soft") instruction set is disclosed in Applicant's co-pending U.S. Patent Application Serial No. 09/418,663 entitled "Method And Apparatus For Managing The Configuration And Functionality Of A Semiconductor Design" filed October 14, 1999, now U.S. Patent No. 6,862,563, which is incorporated herein by reference in its entirety. --